RESEARCH ARTICLE OPEN ACCESS

Implementation of Optimized Reversible Sequential and Combinational Circuits for VLSI Applications

P. Mohan Krishna**, V. G. Santhi Swaroop**, S. Harika*, N. Sravya*, V. Vani*

(** Assistant Professor, Department of Electronics and Communication Engineering, SSCE, Chilakapalem)
(* ug-student, Department of Electronics and Communication Engineering, SSCE, Chilakapalem)

ABSTRACT
Reversible logic has emerged as one of the most important approaches for the power optimization with its application in low power VLSI design. They are also the fundamental requirement for the emerging field of the Quantum computing having with applications in the domains like Nano-technology, Digital signal processing, Cryptography, Communications. Implementing the reversible logic has the advantages of reducing gate counts, garbage outputs as well as constant inputs. In this project we present sequential and combinational circuit with reversible logic gates which are simulated in Xilinx ISE and by writing the code in VHDL . we have proposed a new design technique of BCD Adder using newly constructed reversible gates are based on CMOS with pass transistor gates . Here the total reversible Adder is designed using EDA tools. We will analyze the VLSI limitations like power consumption and area of designed circuits.

***Keywords*:** sequential circuits, combinational circuits Reversible logic gates, Xilinx and EDA

I. INTRODUCTION

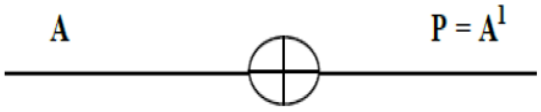
Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Quantum computers are constructed using reversible logic circuits. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. Now-a-days, the electronic systems are an integral part of a human s life. As technology develops, the complexity of the system also increases. This gives rise to increase in power consumption, which is a great issue faced by the world today. One of the causes for high power dissipation is rapid switching of internal signals. Almost all the electronic systems are designed using conventional logic gates, which are irreversible. For each computation in these systems some information (bits) is lost or erased. In 1961, Landauer showed that for each lost bit, a heat of KT ln 2 joules is being generated, where K (1.38x10-23 J/K) is Boltzmann s constant and T is temperature at which computation takes place. According to Moore s law, there is an exponential growth in the heat generated due to information loss, which will reach an intolerable amount in the recent decades. This heat dissipation reduces the performance and lifetime of the circuits.

In this paper we design combinational and sequential circuits using reversible logic gates using Xilinx ISE tool and 8 bit adder circuit was designed using microwind tool.

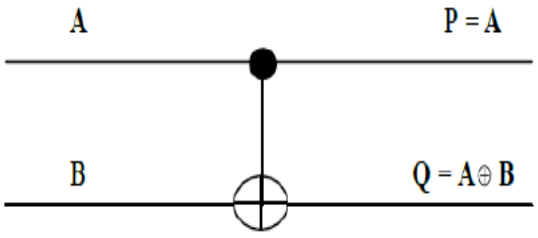
II. REVERSIBLE LOGIC GATES

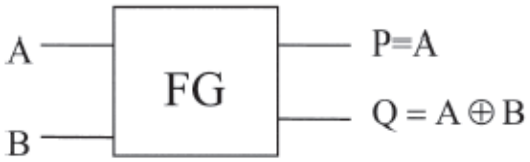
The simplest Reversible gate is NOT gate and is a 1*1 gate. Controlled NOT (CNOT) gate is an example for a 2*2 gate. There are many 3*3 Reversible gates such as F, TG, PG and TR gate. The Quantum Cost of 1*1 Reversible gates is zero, and Quantum Cost of 2*2 Reversible gates is one. Any Reversible gate is realized by using 1*1 NOT gates and 2*2 Reversible gates, such as V, V+ and FG gate which is also known as CNOT gate.

The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Figure 1.

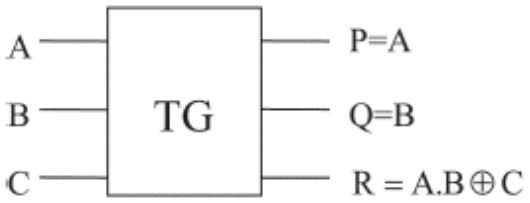


The Reversible 2*2 gate with Quantum Cost of one having mapping input (A, B) to output (P = A, Q = A B) is as shown in the Figure 2.

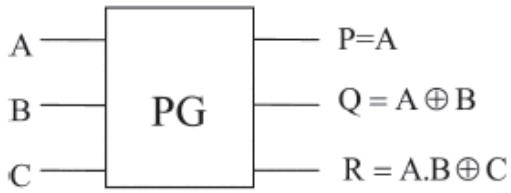




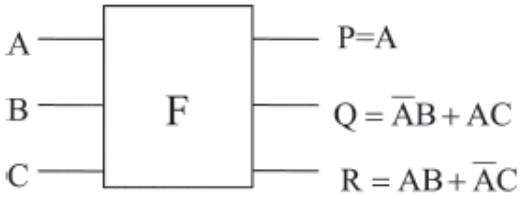
A ToffoliGate (TG) is a 3×3 two-through reversible gate as shown in figure Two-throughmeans two of its outputs are the same as inputs with themapping (A, B, C) to (P = A, Q = B, R = A • B ⊕ C), where A, B, C are inputs and P, Q, R are outputs, respectively. Toffoli gate is one of the most popular reversible gates and has quantum cost of 5 as shown in Figure. The quantum cost of Toffoli gate is 5 as it needs 2 Controlled-V gates, 1 Controlled-V+ gate and 2 CNOT gates to implement it.



P, Q, R are the outputs, respectively. Figure shows the Peres gate and Figure shows the quantum implementation of the Peres gate (PG) with quantum cost of 4. The quantum cost of Peres gate is 4 since it requires 2 Controlled-*V*+ gates, 1 Controlled-V gate and 1 CNOT gate in its design. In the existing literature, among the 3 * 3 reversible gate, Peres gate has the minimum quantum cost.



A Fredkin gate is a (3×3) conservative reversible gate, having the mapping (A, B, C) to (P = A, Q = A'B + AC, R = AB + A'C), where A, B, C are the inputs and P, Q, R are the outputs, respectively [Fredkin and Toffoli 1982]. It is called a 3×3 gate because it has three inputs and three outputs.



III. DESIGN OF REVERSIBLE LATCHES

In this section, we present novel designs of reversible latches that are optimized in terms of quantum cost, delay, and the number of garbage outputs

III.1 The SR Latch:

The SR latch can be designed using two cross-coupled NOR gates or two cross-couple NAND gates. The S input sets the latch to 1, while the R input resets the latch to 0.

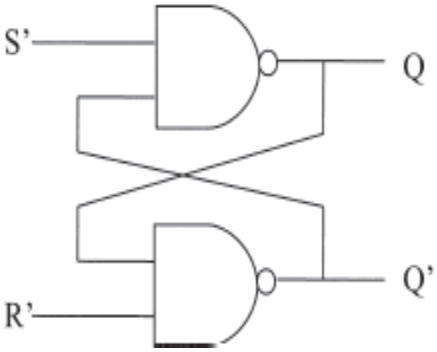


Fig 1: SR Latch

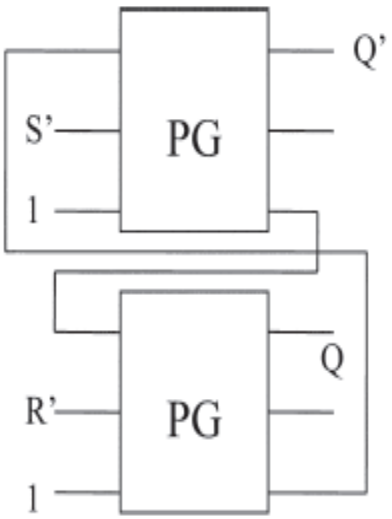


Fig 2 : Pares gate based SR-Latch

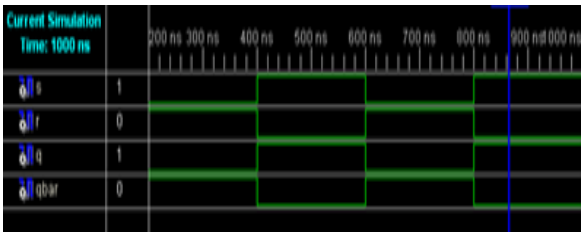


Fig 3: results for SR-Latch

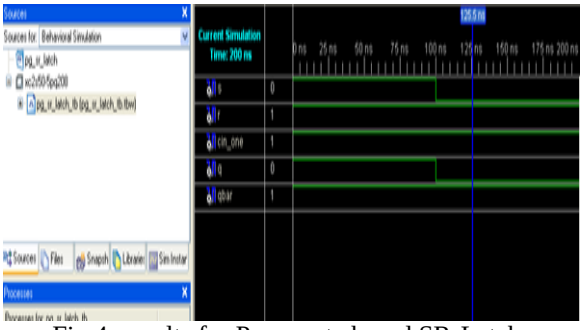


Fig 4: results for Pares gate based SR-Latch

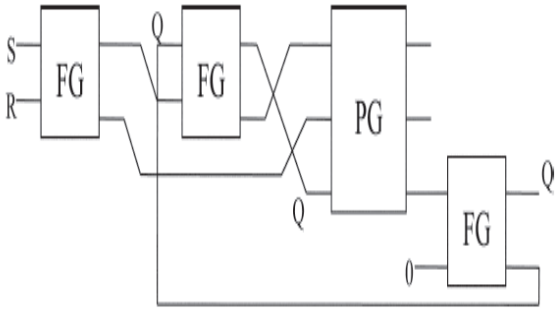
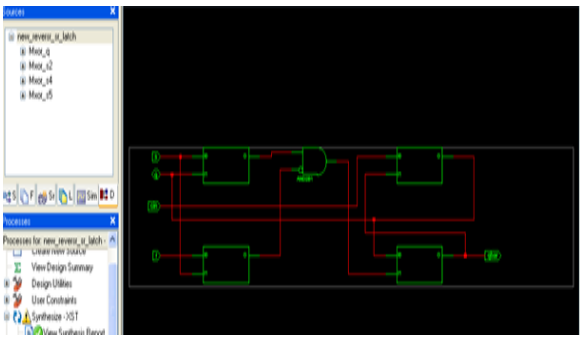


Fig 5: New design of reverse SR-Latch



III.2 The D Latch:

The characteristic equation of the D latch can be written as $Q+ = D\cdot E+ \bar{E}\cdot Q$. When the enable signal(clock) is 1, the value of the input D is reflected at the output that is $Q+ = D$. While, when E = 0 the latchmaintains its previous state, that is $Q+ =$ Q. The characteristic equation of the D latch can be mapped to the Fredkin gate (F) as it matches the template of the Fredkin gate.

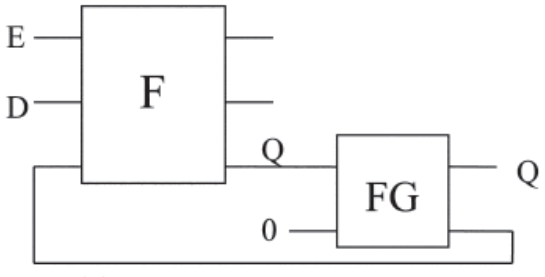


Fig 6: Fredkin based D-Latch

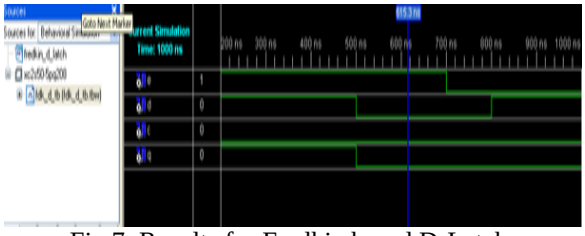


Fig 7: Results for Fredkin based D-Latch

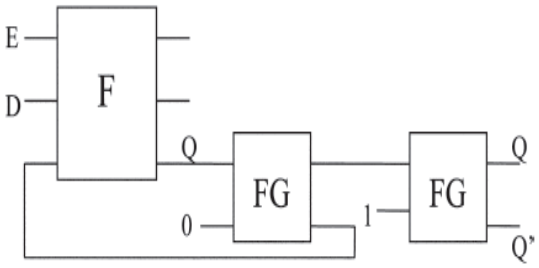


Fig 8: Reversible D-Latch with Q and Q'

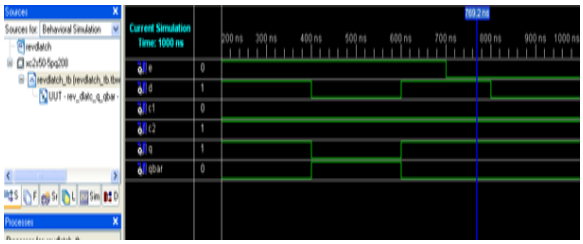


Fig 9: Results for reversible D-Latch with Q and Q'

III. 3 The T Latch:

The characteristic equation of the T latch can bewritten as $Q+ = (T\cdot Q)\cdot E+\bar{E}\cdot Q$. But the same result can also be obtained from $Q+ = (T\cdot E)\oplus Q$. The T(toggle) latch is a complementing latch which complements its value when T = 1, that is when T = 1 and E = 1 we have $Q+ =$ Q'. When T = 0, the T latch maintains its state and we have no change in the output. The T latch characteristic equation can be directly mapped to the Peres gate and the fanout at output Q can be avoided by cascading the Feynman gate. The design has the quantum cost of 5, delay of 5 1 and requires 2 garbage outputs.

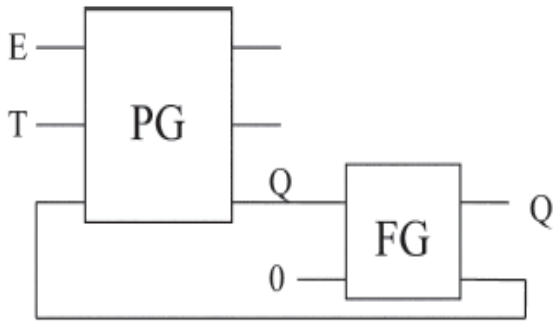


Fig 10: Peres gate based T Latch

Fig 11: Results Peres gate based T Latch

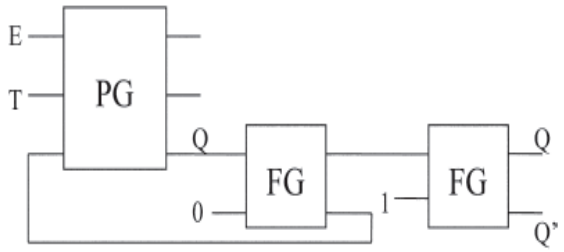


Fig 12:reversible Peres gate based T Latch with Q and Q'

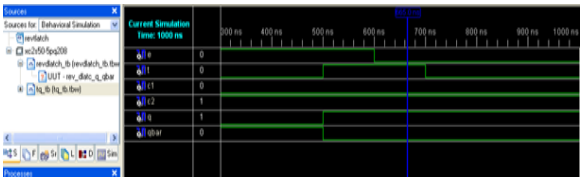


Fig 13 :Results for reversible Peres gate based T Latch with Q and Q'

III.4 DESIGN OF THE REVERSIBLE MASTER-SLAVE FLIP-FLOPS:

The reversible master-slave flip-flops were first presented in Thapliyal et al. in which the authors had used the strategy of using one latch as amaster and the other latch as a slave to design the reversible flip-flops. The same strategy was followed in Rice, Thapliyal and Vinod , and Chuang andWang . The proposed work is also based on the same strategy and the goal is to optimize the quantum cost and the delay of the flip-flops along with the garbage outputs. All the existing reversible master-slave flip-flop designs require the clock to be inverted for use in the slave latch. The proposed masterslave flip-flops designs have a special characteristic of not requiring the clock to be inverted for use in the slave latch. This is because as they use the negative enable D latch as the slave latch, thus no clock inversion is required.

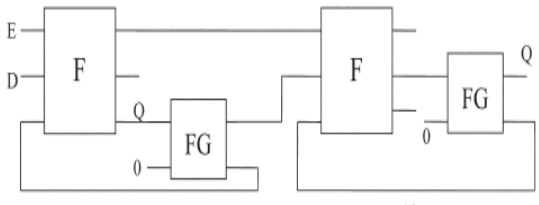
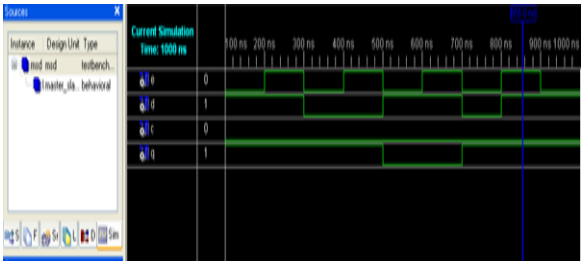


Fig 14:Reversible master slave d flipflop



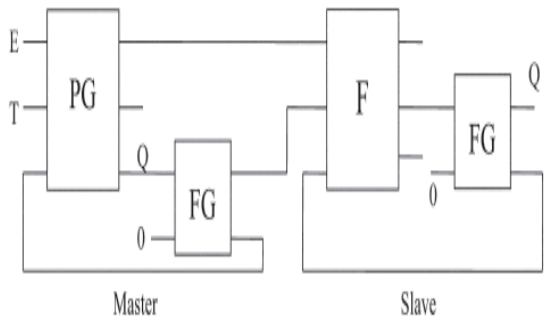
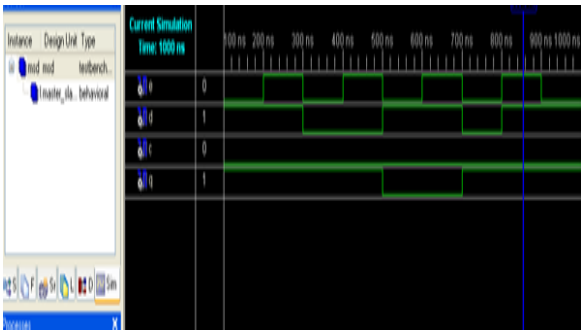


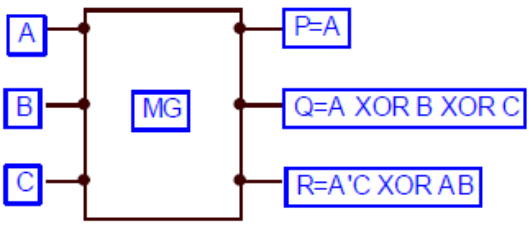
Fig 15 : Reversible master slave T-flip flop

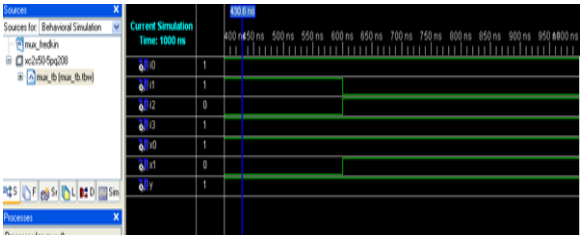


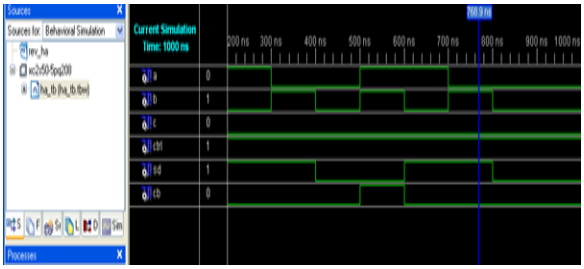
IV. DESIGN OF REVERSIBLE COMBINATIONAL CIRCUITS:

IV.1 MUX Gate:

the pictorial representation of 3×3 reversible gate called MUX (MG) Gate. It is a conservative gate havig three inputs (A, B, C) and three outputs (P, Q, R). The outputs are defined by P=A, Q=A XOR B XOR C and R= A□ C XOR AB. The hamming weight of its input vector is same as the hamming weight of its output vector and its Quantum cost is 4.







IV.2 Frdkingated based fanout circuit:

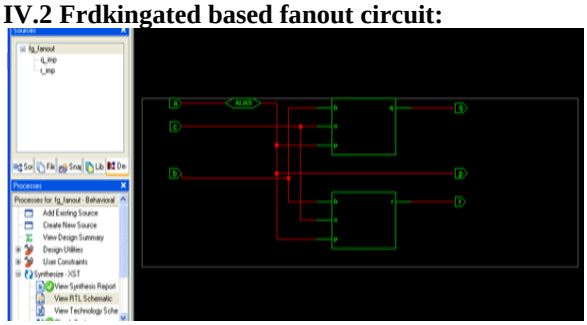
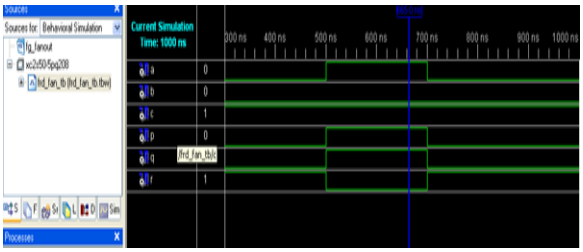


Fig 16: Fanout circuit



IV.3 Fredkin gate based asynchronous reset circuit:

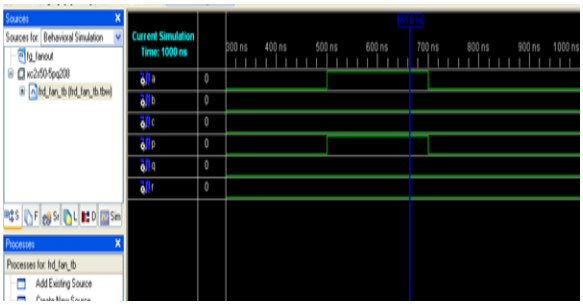


Fig 17 : Results for asynchronous reset circuit

IV.4 Half adder:

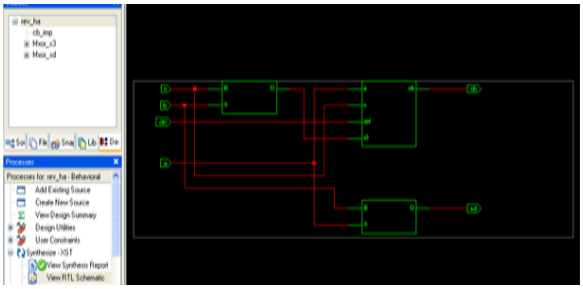


Fig 18 : half adder circuit

IV.5 Full adder:

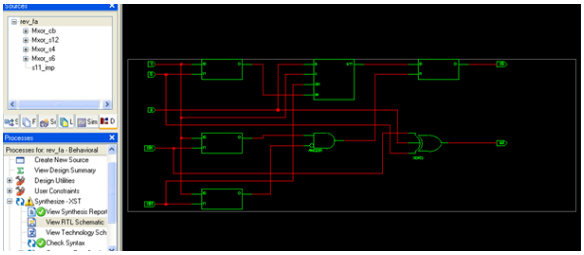
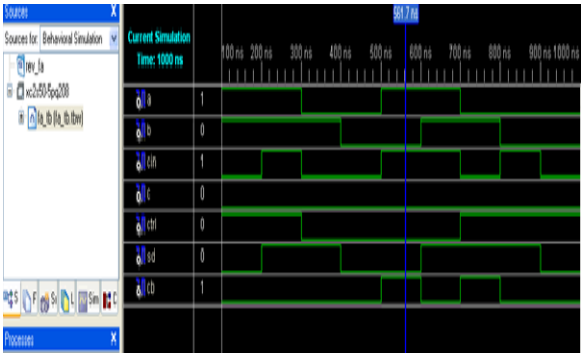


Fig 19 : full adder circuit



IV.6 Subs tractor circuit:

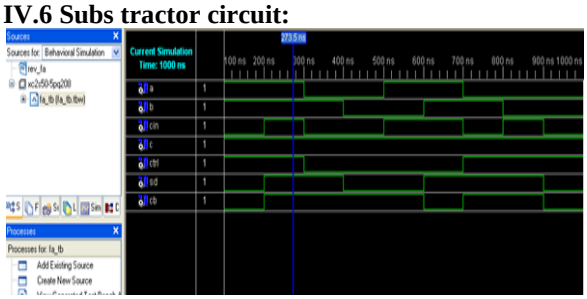


Fig 20 : results for subs tractor circuit

IV.7 Feynman gate used as buffer and not gate:

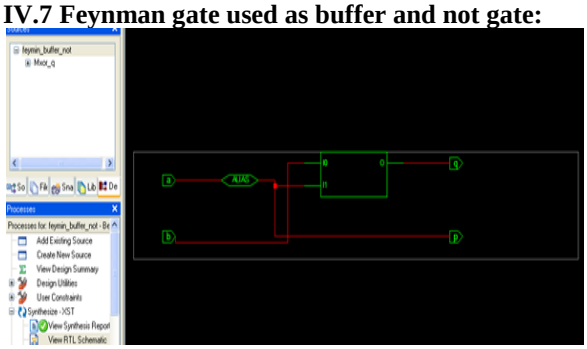
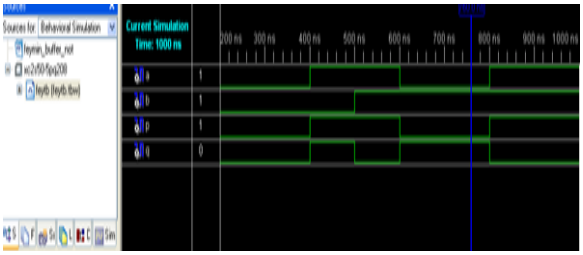


Fig 21: results for buffer and not gate



IV.8 Half adder /subtractor circuit :

Here the circuit was designed using Dsch 2.0 and microwind tool .

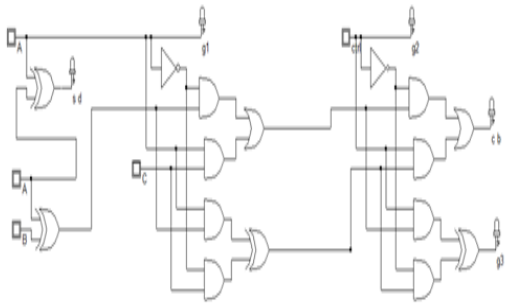


Fig 22: circuit for half adder/subtractor circuit.

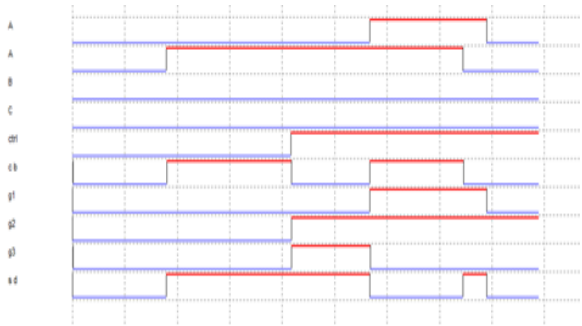


Fig 23: results for half adder/sbtractor circuit

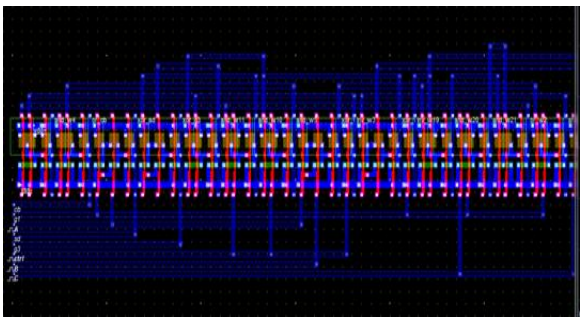


Fig 24: layout for half adder/sbtractor circuit

IV.9 Full adder / subtractor:

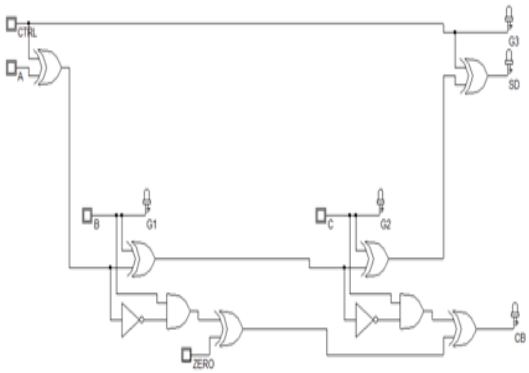


Fig 23 : circuit for full adder/subtrator

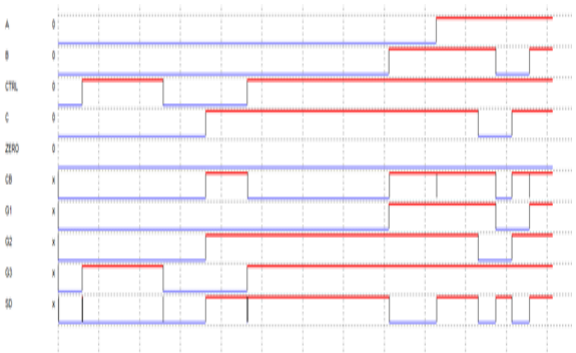


Fig 24: results for full adder/subtrator.

IV.10 8bit full adder /subtracor:

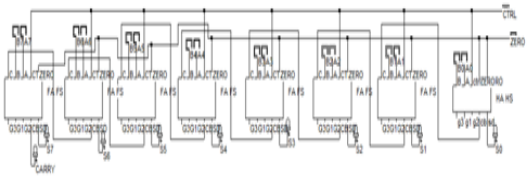


Fig 25: 8bit full adder/subtrator.

V. CONCLUSION

In this work we have presented novel designs of reversible latches and flipflops, which are being optimized in terms of quantum cost, delay, and garbage outputs. The present work differs from the existing approaches in the literature that have optimized the reversible sequential circuit designs in terms of number of reversible gates and garbage outputs. We have also discussed the new designs of reversible D latch and D flip-flop.

In this paper we designed sequential and combinational circuit in reversible logic circuits for

high performance and low quantum cost for vlsi applications.

REFERENCES

[1] BANERJEE, A. AND PATHAK, A. 2007. On the synthesis of sequential reversible circuit.
[2] FRANK, M. 2005b. Introduction to reversible computing: motivation, progress, and challenges.
[3] .”Design of low power arithmetic unit based on reversible logic” in International Journal of VLSI and signal processing applications,
[4] ”A novel design of reversible serial and parallel adder/subtractor” in International journal of engineering science and technology.
[5] Low power reversible parallel binary adder/subtractor by Rangaraju H.G, Venugopal U, Muralidhara K.N, Raja K.B.
[6] ”Optimal design of a reversible full adder” in International Journal of unconventional computing by Yvan Van Rentergen and Alexis De Vos.
[7] T. Toffoli, “Reversible Computing”, Tech Memo MIT/LCS/TM-151, MIT Laboratory for Computer Science, 1980
[8] R. P. Feynman, “Quantum Mechanical Computers”, Optic News, Vol.11, pp.11-20, February 1985
[9] Devendra Goyal, Vidhi Sharma, “VHDL Implementation of Reversible Logic Gates”, International Journal of Advanced Technology and Engineering Research, Vol.2, Issue.3, pp.157-163, May 2012